

AMENDMENTS TO THE CLAIMS

The following claim listing is to replace all previous claim listings. Amendments to the claims are illustrated through strikethrough (for deleted matter) and underlining (for added matter).

CLAIM LISTING

1. (currently amended): A method comprising:
issuing a cache residency test instruction for a set of data; and
determining with a processor unit using the issued cache residency test instruction if the set of data resides in a cache memory that is communicatively coupled to the processor unit;

establishing a relative amount of time to access the set of data by the processor unit; and

communicating a result of the determining to software being executed on the processor unit.

2. (original): A method as described in claim 1, wherein the determining further comprises:

querying whether the set of data resides in the cache memory; and
receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory.

1 3. (original): A method as described in claim 1, wherein the software is
2 selected from the group consisting of an operating system and an application.

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4 4. (cancelled).

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6 5. (original): A method as described in claim 1, wherein the set of data
7 is selected from the group consisting of:

8 an instruction for controlling the processor unit; and

9 data for being processed by the processor unit.
10

11
12 6. (original): A method as described in claim 1, wherein the cache
13 memory is selected from the group consisting of:

14 a cache memory for storing an instruction for controlling the processor unit;

15 a cache memory for storing data for being processed by the processor unit;

16 and
17

18 a combination of the forgoing.

19
20 7. (original): A method as described in claim 1, wherein the
21 determining is performed without reading the set of data into the processor unit
22 from the cache memory unit and without writing the set of data from the processor
23 unit into the cache memory.
24
25

1 8. (original): A method as described in claim 1, further comprising:
2 comparing an address of the set data with at least one other address in the
3 cache memory, wherein the cache memory includes a plurality of levels; and
4 indicating, based on the comparing, to the processor unit whether the
5 address of the set of data is included in the cache memory, wherein if the address
6 is included in the cache memory, the indicating indicates at which level of the
7 plurality of levels the address is included.
8

9
10 9. (original): A method as described in claim 1, wherein the cache
11 memory is configured as a semiconductor-based memory.
12

13 10. (original): One or more computer-readable media comprising
14 computer-executable instructions that, when executed, perform the method as
15 recited in claim 1.
16

17 11. (currently amended): A method comprising:
18 querying whether a set of data resides in a cache memory that is
19 communicatively coupled to a processor unit;
20 receiving an indication at the processor unit from the querying which
21 indicates whether the set of data resides in the cache memory; and
22 communicating the indication to an operating system software being
23 executed on the processor unit.
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2 12. (cancelled).

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4 13. (original): A method as described in claim 11, further comprising
5 establishing a relative amount of time to access the set of data by the processor
6 unit based on the indication which indicates whether the set of data resides in the
7 cache memory.
8

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10 14. (original): A method as described in claim 11, wherein the set of
11 data is selected from the group consisting of:

12 an instruction for controlling the processor unit; and
13 data for being processed by the processor unit.
14

15 15. (original): A method as described in claim 11, wherein the cache
16 memory is selected from the group consisting of:

17 a cache memory for storing an instruction for controlling the processor unit;
18 a cache memory for storing data for being processed by the processor unit;
19 and
20 a combination of the forgoing.
21
22

23 16. (original): A method as described in claim 11, wherein the querying
24 and the receiving are performed without reading the set of data from the cache
25

1 memory to the processor unit and without writing the set of data from the
2 processor unit to the cache memory.

3
4 17. (original): A method as described in claim 11, further comprising:
5 comparing an address of the set data with at least one other address in the
6 cache memory, wherein the cache memory includes a plurality of levels; and
7 providing, based on the comparing, an indication to the processor unit of
8 whether the address of the set of data is included in the cache memory, wherein if
9 the address is included in the cache memory, the indication indicates at which
10 the address is included in the cache memory, the indication indicates at which
11 level of the plurality of levels the address is included.

12
13 18. (original): One or more computer-readable media comprising
14 computer-executable instructions that, when executed, perform the method as
15 recited in claim 11.

16
17 19. (currently amended): A method comprising:
18 comparing an address of a set data with at least one other address in a cache
19 memory, wherein the cache memory includes a plurality of levels and is
20 communicatively coupled to a processor unit;
21 providing an indication to the processor unit, based on the comparing
22 whether the address of the set of data is included in the cache memory, wherein if
23 the address is included in the cache memory, the indication indicates at which
24 the address is included in the cache memory, the indication indicates at which
25

level of the plurality of levels the address is included;

establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and

communicating the indication, by the processor unit, to software being executed on the processor unit.

20. (cancelled).

21. (original): A method as described in claim 19, wherein the software is selected from the group consisting of an operating system and an application.

22. (original): A method as described in claim 19, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit;

and

a combination of the foregoing.

23. (original): One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 19.

24. (original): A method comprising:

supplying an address for a set of data to a comparison unit from a processor unit;

comparing with the comparison unit the address for the set of data with an address in the cache memory;

indicating to the processor unit from the comparison unit based on the comparing whether the address of the set of data is included in the cache memory;

establishing based on the indicating of whether the address of the set of data is included in the cache memory a relative amount of time to access the set of data by the processor unit; and

communicating the established relative amount of time to software being executed by the processor unit.

25. (original): A method as described in claim 24, wherein the access to the set of data by the processor unit is selected from the group consisting of:

writing the set of data; and

reading the set of data.

26. (original): A method as described in claim 24, wherein the comparison unit is selected from the group consisting of:

a memory management unit;

a load/store unit; and

1 a cache controller.
2

3 27. (original): A method as described in claim 24, further comprising
4 translating the address of the set of data such that a format of the address of the set
5 of data corresponds with a format of the at least one other address in the cache
6 memory.
7

8 28. (original): A method as described in claim 24, wherein the cache
9 memory includes a plurality of levels, and the indicating indicates at which level
10 of the plurality of levels the address is included.
11

12
13 29. (original): A method as described in claim 24, wherein the set of
14 data is selected from the group consisting of:

15 an instruction for controlling the processor unit; and
16 data for being processed by the processor unit.
17

18
19 30. (original): A method as described in claim 24, wherein the cache
20 memory is selected from the group consisting of:

21 a cache memory for storing an instruction for controlling the processor unit;
22 a cache memory for storing data for being processed by the processor unit;
23 and
24 a combination of the forgoing.
25

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2 31. (original): A method as described in claim 24, wherein the indicating
3 is performed without reading the set of data from the cache memory to the
4 processor unit and without writing the set of data from the processor unit to the
5 cache memory.

6
7 32. (original): A method as described in claim 24, further comprising
8 signaling that the set of data is to be retained in the cache memory based on the
9 comparison.
10

11
12 33. (original): A method as described in claim 24, wherein the cache
13 memory includes a plurality of levels having addresses of sets of data stored in the
14 levels, and wherein the comparing further comprises comparing the address of the
15 set data with the addresses in the plurality of levels.
16

17
18 34. (original): One or more computer-readable media comprising
19 computer-executable instructions that, when executed, perform the method as
20 recited in claim 24.
21

22 35. (currently amended): For use on a processor unit that is
23 communicatively coupled to a cache memory, a cache residency test instruction,
24 executable on the processor unit, which when executed on the processor unit
25

1 configures the processor unit to performs acts comprising:

2 querying whether a set of data resides in the cache memory;

3 receiving an indication from the querying of whether the set of data resides
4 in the cache memory;

5 establishing a relative amount of time to access the set of data by the
6 processor unit, wherein the establishing is based on the indication which indicates
7 whether the set of data resides in the cache memory; and

8 communicating the indication and the relative amount of time to software
9 being executed on the processor unit.
10

11
12 36. (original): A cache residency test instruction as described in claim
13 35, wherein the processor unit is communicatively coupled to a comparison unit,
14 and execution of the cache residency test instruction by the processor unit
15 configures the comparison unit to perform acts including comparing an address of
16 the set of data with at least one other address in the cache memory in response to
17 the querying.
18

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20 37. (cancelled).
21

22 38. (original): A cache residency test instruction as described in claim
23 35, wherein the set of data is selected from the group consisting of:
24 an instruction for controlling the processor unit; and
25

data for being processed by the processor unit.

39. (original): A cache residency test instruction as described in claim 35, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit;

and

a combination of the forgoing.

40. (original): A cache residency test instruction as described in claim 35, wherein the querying and the receiving are performed without reading the set of data from the cache memory to the processor unit and without writing the set of data from the processor unit to the cache memory.

41. (original): A cache residency test instruction as described in claim 35, wherein the processor unit is communicatively coupled to a comparison unit, and execution of the cache residency test instruction by the processor unit configures the comparison unit to perform acts including:

comparing an address, received from the processor unit from the querying, of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

providing an indication, based on the comparing, to the processor unit of

1 whether the address of the set of data is included in the cache memory, wherein if
2 the address is included in the cache memory, the indicating indicates at which
3 level of the plurality of levels the address is included.

4
5 42. (currently amended): For use on a processor unit that is
6 communicatively coupled to a comparison unit that is communicatively coupled to
7 a cache memory, a cache residency test instruction, which when executed on the
8 processor unit, configures the comparison unit to perform acts comprising:
9

10 comparing an address received from the processor unit with an address in
11 the cache memory;

12 providing an indication to the processor unit based on the comparing of
13 whether the address is included in the cache memory; and

14 communicating the indication to an operating system software being
15 executed by the processor unit.
16
17

18 43. (original): A cache residency test instruction as described in claim
19 42, wherein the indication indicates to the processor unit whether the address is
20 included in the cache memory, and if so, at which level of a plurality of levels of
21 the cache memory the address is included.
22

23 44. (original): A cache residency test instruction as described in claim
24 42, wherein the cache memory is selected from the group consisting of:
25

1 a cache memory for storing an instruction for controlling the processor unit;
2 a cache memory for storing data for being processed by the processor unit;
3 and
4 a combination of the forgoing.

5
6 45. (currently amended): A system comprising:
7 a cache memory; and
8 a processor unit communicatively coupled to the cache memory, wherein
9 the processor unit includes a cache residency test instruction that, when executed,
10 configures the processor unit:
11

12 to query whether a set of data resides in the cache memory;
13 to receive an indication from the query of whether the set of data
14 resides in the cache memory;
15 to establish a relative amount of time to access the set of data; and
16 to communicate the indication and the relative amount of time to
17 software being executed on the processor unit.
18
19

20 46. (original): A system as described in claim 45, further comprising a
21 comparison unit, wherein execution of the cache residency test instruction by the
22 processor unit configures the comparison unit to compare an address of the set of
23 data with at least one other address of the cache memory in response to the query.
24
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1 47. (cancelled).

2
3 48. (original): A system as described in claim 45, wherein the set of data
4 is selected from the group consisting of:

5 an instruction for controlling the processor unit; and

6 data for being processed by the processor unit.

7
8 49. (original): A system as described in claim 45, wherein the cache
9 memory is selected from the group consisting of:

10 a cache memory for storing an instruction for controlling the processor unit;

11 a cache memory for storing data for being processed by the processor unit;

12 and

13 a combination of the forgoing.

14
15 50. (original): A system as described in claim 45, wherein the cache
16 memory includes a plurality of levels, if the address is included in the cache
17 memory, the indication indicates at which level of the plurality of levels the
18 address is included.

19 51. (currently amended): A system comprising:

20 a processor unit;

21 a comparison unit communicatively coupled to the processor unit; and

1 a cache memory communicatively coupled to the comparison unit, wherein
2 the comparison unit is configured:

3 to compare an address received from the processor unit with at least
4 one address in the cache memory; and

5 to provide an indication to the processor unit indicating whether the
6 address is included in the cache memory based on the comparison such that
7 the processor unit is configured to establish a relative amount of time to
8 access a set of data specified by the address.
9

10
11 52. (original): A system as described in claim 51, wherein the
12 comparison unit is selected from the group consisting of:

13 a memory management unit (MMU);
14 a load/store unit; and
15 a cache controller.
16

17
18 53. (original): A system as described in claim 51, wherein the set of data
19 is selected from the group consisting of:

20 an instruction for controlling the processor unit; and
21 data for being processed by the processor unit.
22

23
24 54. (original): A system as described in claim 51, wherein the cache
25 memory is selected from the group consisting of:

1 a cache memory for storing an instruction for controlling the processor unit;
2 a cache memory for storing data for being processed by the processor unit;
3 and
4 a combination of the forgoing.

5
6 55. (original): A system as described in claim 51, wherein the cache
7 memory includes a plurality of cache memory levels, the comparison unit is
8 configured to provide an indication which indicates if the address of the set of data
9 is included in the cache memory, at which level of the plurality of levels the
10 address of the set of data is included.
11

12
13 56. (currently amended): A processor chip comprising
14 a processor unit having a coupling for communicatively coupling the
15 processor unit to a cache memory, wherein:
16

17 the processor unit includes storage for a cache residency test
18 instruction; and

19 an execution of the cache residency test instruction with the
20 processor unit configures the processor unit to determine if a set of data
21 resides in the cache memory, establish a relative amount of time to access
22 the set of data, and communicate a result of the determination and the
23 relative amount of time to software being executed on the processor unit.
24
25

1 57. (original): A processor chip as described in claim 56, further
2 comprising a second processor unit having:

3 a coupling for communicatively coupled the second processor unit to
4 the cache memory;

5 storage for a second cache residency test instruction; and

6 an execution of the second cache residency test instruction with the
7 second processor unit configures the second processor unit to determine if a
8 set of data resides in the cache memory and communicate a result of the
9 determination to software being executed on the second processor unit.
10

11
12 58. (original): A processor chip as described in claim 56, wherein the set
13 of data is selected from the group consisting of:

14 an instruction for controlling the processor unit; and
15 data for being processed by the processor unit.
16

17
18 59. (original): A processor chip as described in claim 56, wherein the
19 cache memory is selected from the group consisting of:

20 a cache memory for storing an instruction for controlling the processor unit;

21 a cache memory for storing data for being processed by the processor unit;

22 and

23 a combination of the forgoing.
24
25

1 60. (original): A processor chip as described in claim 56, wherein the
2 cache memory is selected from the group consisting of:

3 a cache memory located on the processor chip;

4 a cache memory located off the processor chip; and

5 a combination of the forgoing.

6
7 61. (original): A processor chip as described in claim 56, wherein the
8 cache memory is configured as a semiconductor-based memory.

9
10
11 62. (original): A processor chip as described in claim 56, wherein the
12 software is selected from the group consisting of an operating system and an
13 application.

14
15 63. (currently amended): A computing device comprising:
16 a storage device; and
17 a processor chip, communicatively coupled to the storage device, and
18 including:

19 a cache memory; and

20 a processor unit communicatively coupled to the cache memory,
21 wherein the processor unit includes storage for a cache residency test
22 instruction that, when executed by the processor unit, configures the
23 processor unit to determine if a set of data resides in the cache memory and
24
25

1 to communicate a result of the determination to an operating system
2 ~~software~~ being executed on the processor chip.

3
4 64. (currently amended): A computing device as described in claim 63,
5 wherein the processor chip further comprises a second processor unit
6 communicatively coupled to the cache memory, wherein the second processor unit
7 includes storage for a second cache residency test instruction that, when executed
8 by the second processor unit, configures the second processor unit to determine if
9 a set of data resides in the cache memory and to communicate a result of the
10 determination to the operating system ~~software~~ being executed on the processor
11 chip
12

13
14 65. (original): A computing device as described in claim 63, wherein the
15 set of data is selected from the group consisting of:

16
17 an instruction for controlling the processor unit; and
18 data for being processed by the processor unit.
19

20 66. (original): A computing device as described in claim 63, wherein the
21 cache memory is selected from the group consisting of:

22 a cache memory for storing an instruction for controlling the processor unit;
23 a cache memory for storing data for being processed by the processor unit;
24

25 and

1 a combination of the forgoing.

2
3 67. (original): A computing device as described in claim 63, wherein the
4 cache memory is configured as a semiconductor-based memory.

5
6 68. (cancelled).